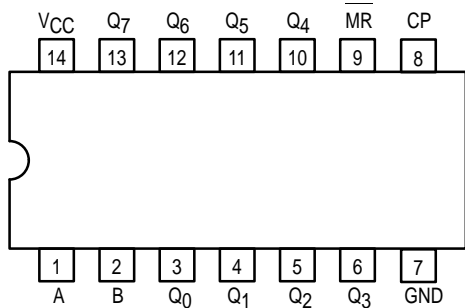![Motorola logo] **MOTOROLA**

SERIAL-IN PARALLEL-OUT SHIFT REGISTER

The SN54/74LS164 is a high speed 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with the LOW to HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL products.

- Typical Shift Frequency of 35 MHz
- Asynchronous Master Reset
- Gated Serial Data Input
- Fully Synchronous Data Transfers
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts

CONNECTION DIAGRAM DIP (TOP VIEW)

Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8
V_{CC}	Q_7	Q_6	Q_5	Q_4	$\overline{MR}$	CP

Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7
A	B	Q_0	Q_1	Q_2	Q_3	GND

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

SN54/74LS164

SERIAL-IN PARALLEL-OUT SHIFT REGISTER

LOW POWER SCHOTTKY
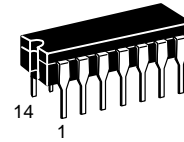
J SUFFIX
CERAMIC
CASE 632-08

N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL

V_{CC} = PIN 14
GND = PIN 7

PIN NAMES

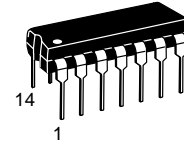|		LOADING (Note a)	
		HIGH	LOW
A, B	Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$Q_0 - Q_7$	Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
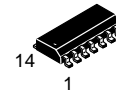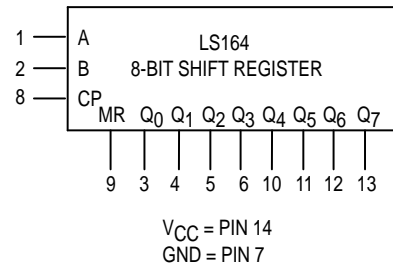
SN54/74LS164

LOGIC DIAGRAM

V$_{CC}$ = PIN 14
GND = PIN 7
◯ = PIN NUMBERS
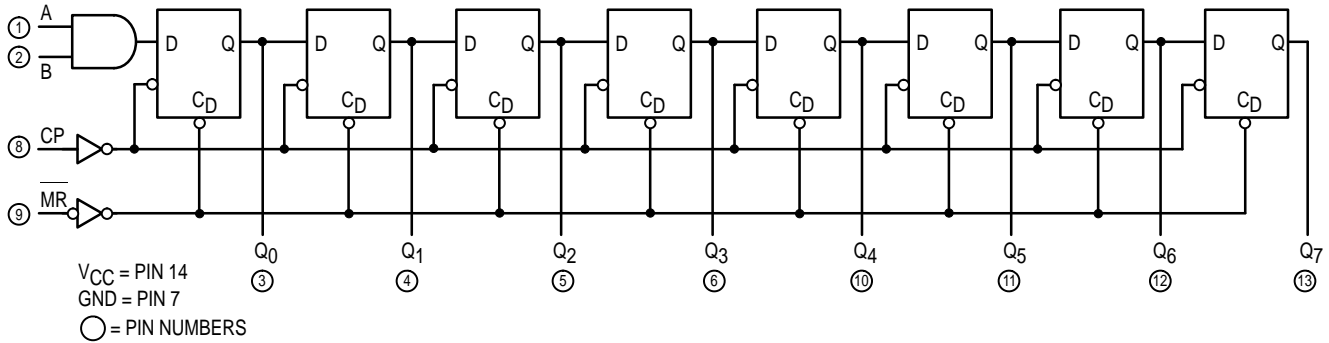
FUNCTIONAL DESCRIPTION

The LS164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q$_0$ the logical AND of the two data inputs (A•B) that existed before the rising clock edge. A LOW level on the Master Reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	A	B	Q$_0$	Q$_1$–Q$_7$
Reset (Clear)	L	X	X	L	L – L
Shift	H	l	l	L	q$_0$ – q$_6$
	H	l	h	L	q$_0$ – q$_6$
	H	h	l	L	q$_0$ – q$_6$
	H	h	h	H	q$_0$ – q$_6$

L (l) = LOW Voltage Levels
H (h) = HIGH Voltage Levels
X = Don't Care
q$_n$ = Lower case letters indicate the state of the referenced input or output one
    set-up time prior to the LOW to HIGH clock transition.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V$_{CC}$	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T$_A$	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I$_{OH}$	Output Current — High	54, 74			−0.4	mA
I$_{OL}$	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS164

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5				
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				27	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
f_{MAX}	Maximum Clock Frequency	25	36		MHz	
t_{PHL}	Propagation Delay MR to Output Q		24	36	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay Clock to Output Q		17 21	27 32	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_W	CP, MR Pulse Width	20			ns	
t_s	Data Setup Time	15			ns	V_{CC} = 5.0 V
t_h	Data Hold Time	5.0			ns	
t_{rec}	MR to Clock Recovery Time	20			ns	

SN54/74LS164

AC WAVEFORMS

*The shaded areas indicate when the input is permitted to change for predictable output performance.
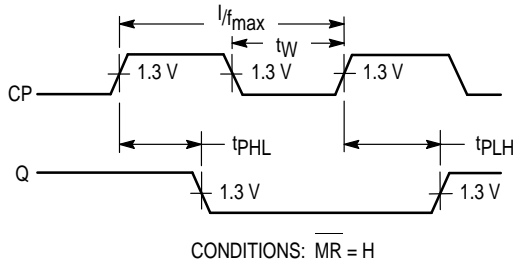
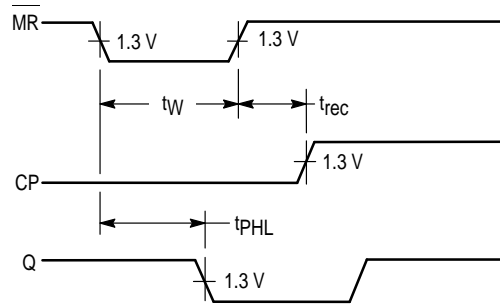

**Figure 1. Clock to Output Delays
and Clock Pulse Width**

**Figure 2. Master Reset Pulse Width,
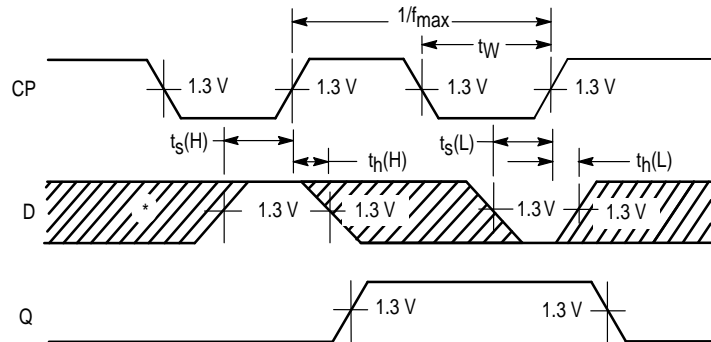Master Reset to Output Delay and
Master Reset to Clock Recovery Time**

Figure 3. Data Setup and Hold Times